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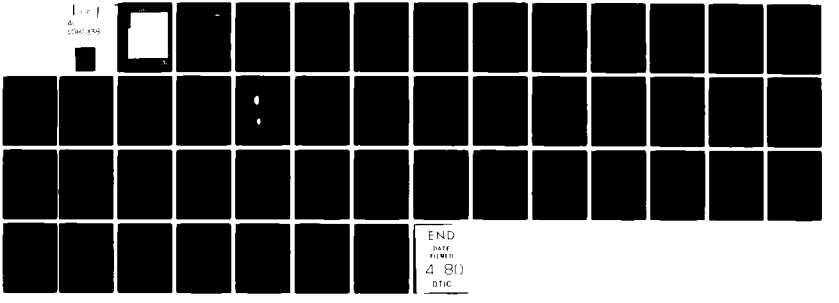

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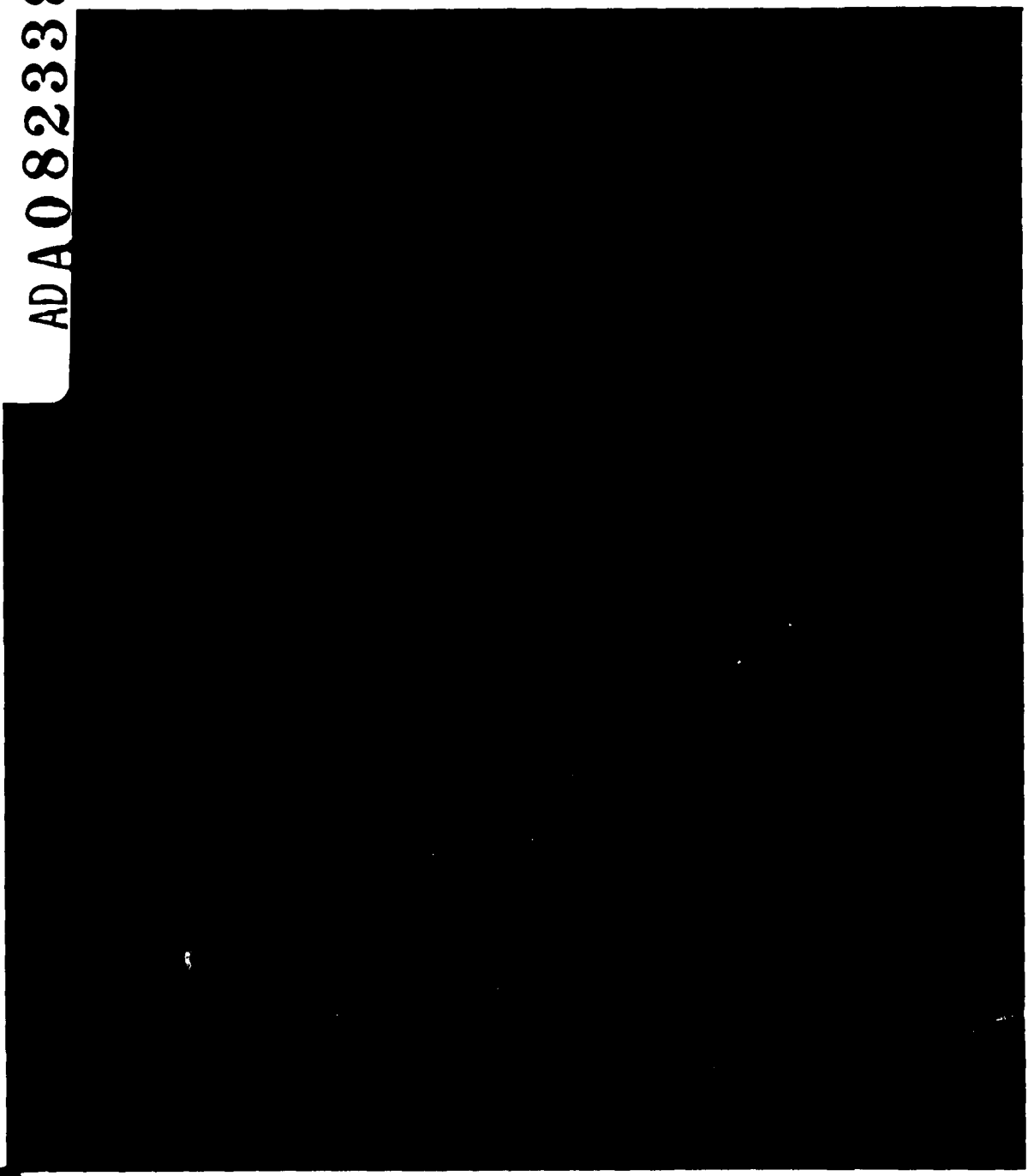

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The goal of this research program is to demonstrate processing techniques which can eliminate the need for high temperature thermal cycling of silicon wafers in fabricating very large scale integrated (VLSI) devices. Maintaining low temperatures for all processing reduces plastic deformation, diffusion and autodoping problems which would limit the application of submicron geometry design rules. Pulsed electron beam surface heating of the top micron of material is being investigated for annealing of ion-implantation damage and

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epitaxial regrowth of low temperature chemical-vapor-deposition (CVD) polycrystalline silicon films. Research to date has demonstrated the epitaxial regrowth of 0.1 to 0.5 micron films deposited at 600 to 800°C, with and without etching the native oxide on the substrate. Annealing of ion-implantation damage for boron and arsenic implants in the range 10^{12} to 10^{16} ions/cm^2 dose has been demonstrated with a combination of low temperature (550°C) furnace and pulse treatments. Diodes have been fabricated by pulse techniques with characteristics comparable to furnace annealed devices. Research planned in the next 6 months will stress characterization of diodes and transistors processed by pulsed techniques.

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REPORT SUMMARY

1.1 PROGRAM OBJECTIVES

The goal of this program is to reduce the maximum temperature used in processing large scale integrated circuits by using large area pulsed electron beams. Specifically, the program is to demonstrate: (1) that a thin silicon film can be deposited at low temperatures with impurity levels consistent with requirements for submicron devices, (2) that the structure of this film can be changed from amorphous or polycrystalline to single crystal through pulsed irradiation by electron beams, (3) that ion implanted junctions can be annealed by pulsed technology, and (4) that an operational device typical of very large scale integrated (VLSI) technologies can be fabricated by these techniques.

1.2 TECHNICAL CONSIDERATIONS

Existing technology for the fabrication of integrated circuits uses high temperatures (over 1000°C) for the growth of epitaxial films[1] and annealing of ion implantation damage[2]. Plastic deformation of the substrate and diffusion from previously deposited layers occurs at these temperatures, but the effect is not limiting until devices employ submicron dimensions[3]. This program is to demonstrate that epitaxial films can be formed at low temperatures and that active device junctions formed by ion implantation can be annealed without heating the substrate to high temperatures. The program is also to demonstrate that the motion of dopants in both processes is restricted.

1.3 GENERAL METHODS

High temperature furnace processing steps are replaced by pulsed electron beam surface heating[4]. Through control of beam fluence and particle energy this electron beam can be used to heat (or melt) up to 1.0 micrometer of silicon, heating the bulk of the substrate no more than 10°C. Short period thermal gradients cause epitaxial crystal regrowth in the heated surface material to anneal ion implantation damage and recrystallize deposited films. Combined with a low temperature deposition technique to

put down an appropriate film, the technique described can form a lightly doped high quality epitaxial film over a heavily doped substrate. To anneal ion implanted junctions for small scale active devices, a process has been developed based upon a multiple step, low temperature furnace and low fluence pulsed electron beam treatment.

1.4 TECHNICAL RESULTS/CONCLUSIONS

SUMMARY

This program has:

- Identified a optimum low temperature film deposition process
- Demonstrated pulsed electron beam epitaxial regrowth of this deposited film
- Demonstrated annealing of varying dose ion implanted junctions
- Discovered that oxygen does not diffuse away from a 15-20Å buried SiO_2 interface within pulse melted silicon.

FILM DEPOSITION

Polycrystalline chemical-vapor-deposition (CVD) of films has been identified as the optimum technique for low temperature, high purity deposition of silicon. Low-pressure-chemical-vapor-deposition (LPCVD) of films was tested on different substrates including (111) CZ silicon doped with arsenic (0.003 ohm-cm) or antimony (0.02 ohm-cm). Additional LPCVD films were prepared on (100) CZ silicon boron doped (1.0 ohm-cm) wafers with and without a junction on the surface formed by ion implantation ($1x10^{16}$ As/cm^2) and annealed prior to deposition. The contamination levels of these LPCVD films, measured by secondary ion mass spectroscopy (SIMS) analysis, is shown in Figures 2-4 and 2-6. The films deposited at 625^{o}C show about the same concentration of H, O, and N as the substrate and an increase in carbon content by a factor of four to five. Films deposited at 550^{o}C, Figure 2-6, also show an increase in hydrogen content. Note that the dopant profile has a very sharp interface in low temperature deposits. Conventional epitaxial silicon films deposited by CVD, Figure 2-5, show no increase in any contaminant detected. This will dictate the choice of deposition for future experiments to form devices.

PULSED EPITAXY

Excellent pulsed epitaxial regrowth of 0.3 to 0.4 μm LPCVD polycrystalline films was demonstrated with low autodoping. Samples were irradiated with a 100 ns pulsed electron beam at a fluence between 0.9 and 1.1 J/cm^2. This range of pulsed beam parameters bracketed the threshold for epitaxial growth as determined by reflected high-energy electron diffraction (RHEED) analysis (Figure 2-2). The samples on arsenic doped wafers were analyzed by secondary ion mass spectroscopy (SIMS) and show a more abrupt junction than was achieved by conventional CVD (Figure 2-3). The antimony doped samples were profiled by capacitance-voltage analysis and also showed an abrupt junction (Figure 2-9). The results are consistent with a simple model for regrowth from the liquid phase.

A key experiment designed to show improved control of dopant motion in pulsed epitaxy, through the use of amorphous LPCVD films, could not be completed because high-quality pure silicon amorphous films were not obtained by direct deposition. The experiment was changed, and polycrystalline films from the previous work were heavily damaged (rendered amorphous) by ion implantation of silicon. These films were melted at lower fluence. Further analysis is underway to determine the motion of the dopant.

OXIDE INTERFACE

All LPCVD films were deposited on cleaned substrates without etching the native oxide film (15-20Å thick) in the reactor. An oxide etch at 1200°C is normally used in CVD epitaxy, but it is inconsistent with the low temperature processing goals of this program and the LPCVD equipment. The original oxide interface can be seen after LPCVD in Figure 2-4, a SIMS depth profile analysis. The width of this interface appears broadened due to ion sputtering. Note that increased levels of carbon and nitrogen are also present at this interface. After pulsing, carbon, nitrogen and the arsenic dopant have diffused away from this region but not oxygen. The melt depth has extended into the substrate as inferred from the arsenic profile. The implication of the remaining oxygen is that either epitaxial regrowth has occured through a thin oxide interface, or that the oxide layer became discontinuous on a microscopic scale to permit epitaxial growth of the film as it solidified. The stability of this oxide interface is an important new result.

PULSED ANNEALING

Annealing of ion implantation damage was demonstrated for boron implants at 25 keV for doses between 10^{12} to 10^{15} ions/cm^2 into (100) phosphorus doped silicon. Experiments discussed in Section 3 of this report compare different annealing schedules: (a) 550°C for 1 hour, (b) step a plus 950°C for 15 minutes, (c) step a plus one electron beam pulse, and (d) this same pulse treatment alone. The combination of furnace and pulse anneal yielded sheet resistances nearly the same as an optimized two step furnace (only) anneal encountered in many processing situations. Mesa etched diode characteristics of pulsed and furnace annealed material are also similar. Preliminary measurements of sheet resistance, dopant distribution, and diode characteristics are given in Figures 3-2 and 3-3 and in Tables 3-1 through 3-3. As reported previously, the uniformity of PEBA processing (as measured by sheet resistance) is presently better than ±4 percent for a 3-inch wafer and can be improved in the future.

1.5 PROGRAM FUTURE DIRECTIONS

The experiments on pulsed electron beam liquid epitaxy (PEBLE) have been successfully completed (Task 1) for measurements of physical parameters. However, because LPCVD deposits were not amorphous, and because such amorphous films may lead to better control of melt depth and dopant distribution, one further experiment is planned. This test will use ion implanted films (high dose Si) to determine the effect on melt depth experimentally.

Pulsed electron beam annealing (PEBA) has been most successful with a combination of pulse and low temperature furnace treatment. It is expected that this study will define and optimize the process for a variety of arsenic, boron, and phosphorus implantation schedules. The regrowth rate of ion implantation damaged silicon as a function of the number of nonmelting pulses from an intense electron beam will be determined. However, it may be better to use one pulse with a pre- and post-furnace treatment. The principal effort on this program in the next six months will be the measurement of the electrical properties of the silicon layers formed by pulse epitaxy or by pulse annealing. Mesa diodes will be used to characterize the annealing by C-V measurements. Other planned devices include junction FET's and/or Schottky barrier FET's. Experiments for testing geometrical effects, such as lateral dopant motion and edge effects, are planned using a series of implanted resistors from 1 to 50 micrometers wide, and an implanted interdigitated pattern 2.5 micrometers wide with 3.5 micrometer spacing. Masks for these tests and devices have been fabricated and are described in Section 4. It is expected that these measurements will extend to the end of the contract.

SECTION 2
PULSED EPITAXIAL REGROWTH

2.1 OBJECTIVE OF TASK 1, FILM DEPOSITION

The objective of this task is to deposit on a silicon substrate a silicon film, at low temperatures, of high purity with appropriate doping and structure for task 2, pulsed epitaxy. Additionally, conventional CVD epitaxial films will be prepared for comparison. All films are to be characterized for structure, doping profiles, and impurities or defects.

In this context, low temperature implies that the wafer is not heated to the point where plastic deformation or thermally induced stress will alter the geometry or relative position of the substrate or any film on its surface[3]. Also, the temperature must be kept below the point where diffusion of dopants occurs for a distance equal to the minimum line width for VLSI (about 0.25 micrometer) or the minimum layer thickness. At this time, it appears possible to keep the substrate temperature below 650°C.

These deposited films are to be turned into crystalline silicon used for active device structures. Therefore, the level of impurities is expected to be less than $10^{12}/cm^3$. Appropriate doping levels would be about 1 to 10 ohm-cm. The crystal structure before epitaxial regrowth should be small grain random polycrystalline or amorphous material to increase contrast between pre- and postpulse results.

2.2 OBJECTIVES OF TASK 2, LOW TEMPERATURE REGROWTH

Deposition of epitaxial silicon films on single crystal substrates is easily achieved above 900°C[1] but cannot be achieved at low temperatures such as are desirable in this program. This task is to demonstrate that a chemically pure but poor crystallographic silicon film can be melted and regrown epitaxially without disturbing the dopant pattern in the underlying substrate. The final product must be suitable for making devices. The process is illustrated in Figure 2-1.

The objectives for this tasks are to (1) analyze the pulsed epitaxial requirement for VLSI technology, (2) develop and characterize a pulsed electron beam to meet these requirements, (3) demonstrate pulsed epitaxial regrowth of silicon films, and (4) compare these films to conventional CVD epitaxial structure. These objectives have been met. An additional goal, requiring one further experiment, is to show control of melt depth in amorphous compared to polycrystalline deposits.

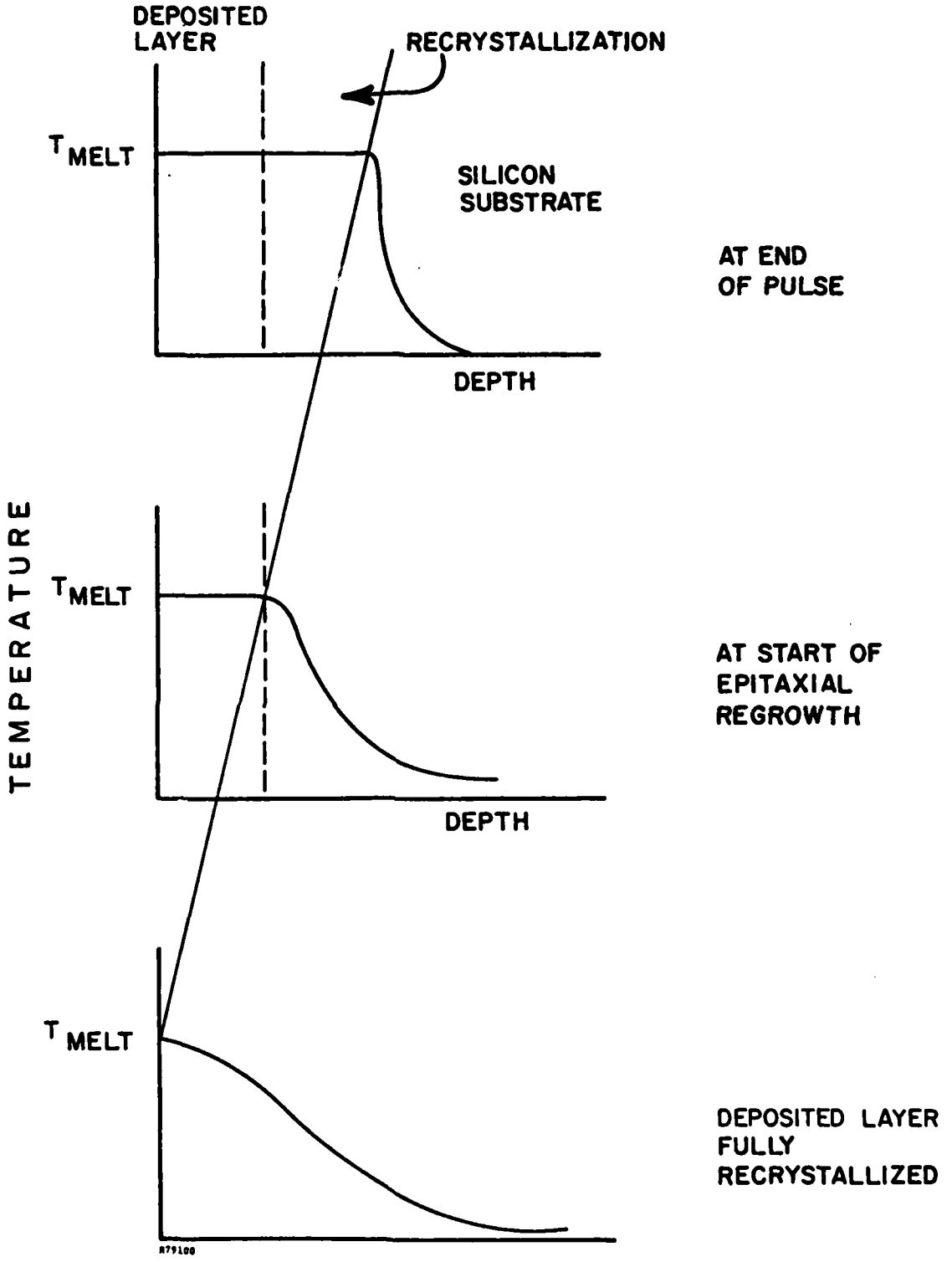


FIGURE 2-1. Thermal-physical model of pulsed electron beam liquid phase epitaxial regrowth of deposited silicon layer.

2.3 ANALYSIS OF DEPOSITED FILMS

Initial experiments on this program[5] demonstrated pulsed epitaxy of 0.1- to 0.6-micrometer-thick, large grain polycrystalline films. The goal of showing reduced autodoping was not achieved because the films were highly doped as deposited. To reduce this problem, a series of films was deposited on silicon substrates by outside vendors at lower temperatures (650°C versus 840°C) than available at Spire Corporation. Suitable films were obtained from Applied Materials, Inc., Hewlett Packard, and Microwave Associates, Inc.

The films deposited at low temperatures were all small grain polycrystalline. They all showed strong diffraction ring patterns for near surface material and no electron channeling pattern. By contrast, the films deposited at higher temperatures at Spire Corporation showed strong preferential orientation of the crystallites by electron diffraction and electron channeling patterns. The difference in structure shows more clearly the reordering occurring after pulse processing.

2.3.1 LPCVD from Applied Materials, Inc.

The first series of experiments used low pressure chemical vapor deposition (LPCVD) apparatus from Applied Materials, Inc. Two types of substrates were furnished, arsenic doped to 0.003 ohm-cm and antimony doped to 0.02 ohm-cm. Both were polished 2-inch o.d. silicon wafers with (111) orientation. The film on each set of substrates was deposited in separate but identical runs in the same reactor. The wafers were etched in buffered HF solution before insertion into the reactor. The reactor was then purged and heated to 628°C. The temperature uniformity was +0°C, -25°C. The film was deposited from pure silane (SiH_4) with no carrier gas at 0.255 torr. Measured deposition rate was 8.5 nm/s. Film thickness was 0.4 micrometer for a 48-minute run. The uniformity, wafer to wafer, was $\pm$4 percent. Dopant was not deliberately added to the gas stream during deposition. Nominal dopant concentration in the film was about $10^{15}/cm^3$ due to autodoping effects.

These films were deposited without completely etching off the oxide surface layer on the substrate. The cleaning procedure used was expected to reduce the oxide thickness to 1.5 to 2.0 nanometers. Complete removal of the oxide would require etching at 1175°C in HCl, which is contrary to the low temperature processing desired. Experiments show that this remaining oxide film does not inhibit epitaxial regrowth from the melt phase.

These films were analyzed by reflected high-energy electron diffraction (RHEED), electron channeling, and scanning electron microscopy (SEM) for structure[6]. They were also analyzed by secondary ion mass spectroscopy (SIMS).[7] The results are shown in Figures 2-2 and 2-3.

In Figure 2-2, before pulsing, strong uniform circular patterns are visible. This is characteristic of small grain (less than 0.5 micrometer) randomly oriented polycrystalline material. Larger grains would produce a spotty nonuniform circular pattern, and preferred orientation would yield a twinned structure[5]. The lines can all be identified from silicon crystal planes. Electron channeling patterns of these films were impossible to obtain before pulsing; attempts yielded uniformly gray exposures. Since a 75-nanometer amorphous Si film on a crystal substrate was sufficient to yield the same results, the grain size of the crystallites must be smaller.

In Figure 2-3, the doping of the film on an arsenic (0.003 ohm-cm) wafer is compared to the postpulse results. The measured curves are SIMS data, and a certain amount of error (rounding) is possible at the interface due to ion sputtering effects. The interface of the original film is very sharp with a change of over three orders of magnitude in dopant concentration in less than 50 nanometers. This is much better than can be achieved in epitaxy by CVD.

The contamination level in this film is shown in Figure 2-4, a SIMS profile of H, C, N, O, and As. Note that nitrogen could be detected better as SiN, and that the profile of hydrogen was extremely noisy and cannot be interpreted. The unetched oxide film at the interface was easily detected, but the width cannot be inferred from this data because sputtering broadens the peak. This interfacial film contained significant amounts of carbon and nitrogen, but the relative concentration, compared to oxygen, cannot be inferred from this data because the detector sensitivity varies between elements. The dip in the Si_4 curve is real, and indicates the relative amount of oxygen at the interface. The data does show that the oxygen and nitrogen content of the polycrystalline film is the same as in the substrate, while the carbon content of the film is about four times that of the substrate. For comparison, a SIMS profile of the same elements in a comparable, conventional CVD epitaxial film (Figure 2-5) shows no change in H, C, N, or O between the film and substrate. Note that the arsenic profile does not show as sharp a junction in Figure 2-5 compared to Figure 2-4 (before pulse) because of outdiffusion from the substrate into the film during epitaxial growth at 1150°C.

BEFORE AFTER

FIGURE 2-2. RHEED patterns of 0.4-micrometer LPCVD material before and after pulsed electron beam irradiation, showing a change in crystal structure from small-grain random polycrystalline material to a single crystal with epitaxial orientation.

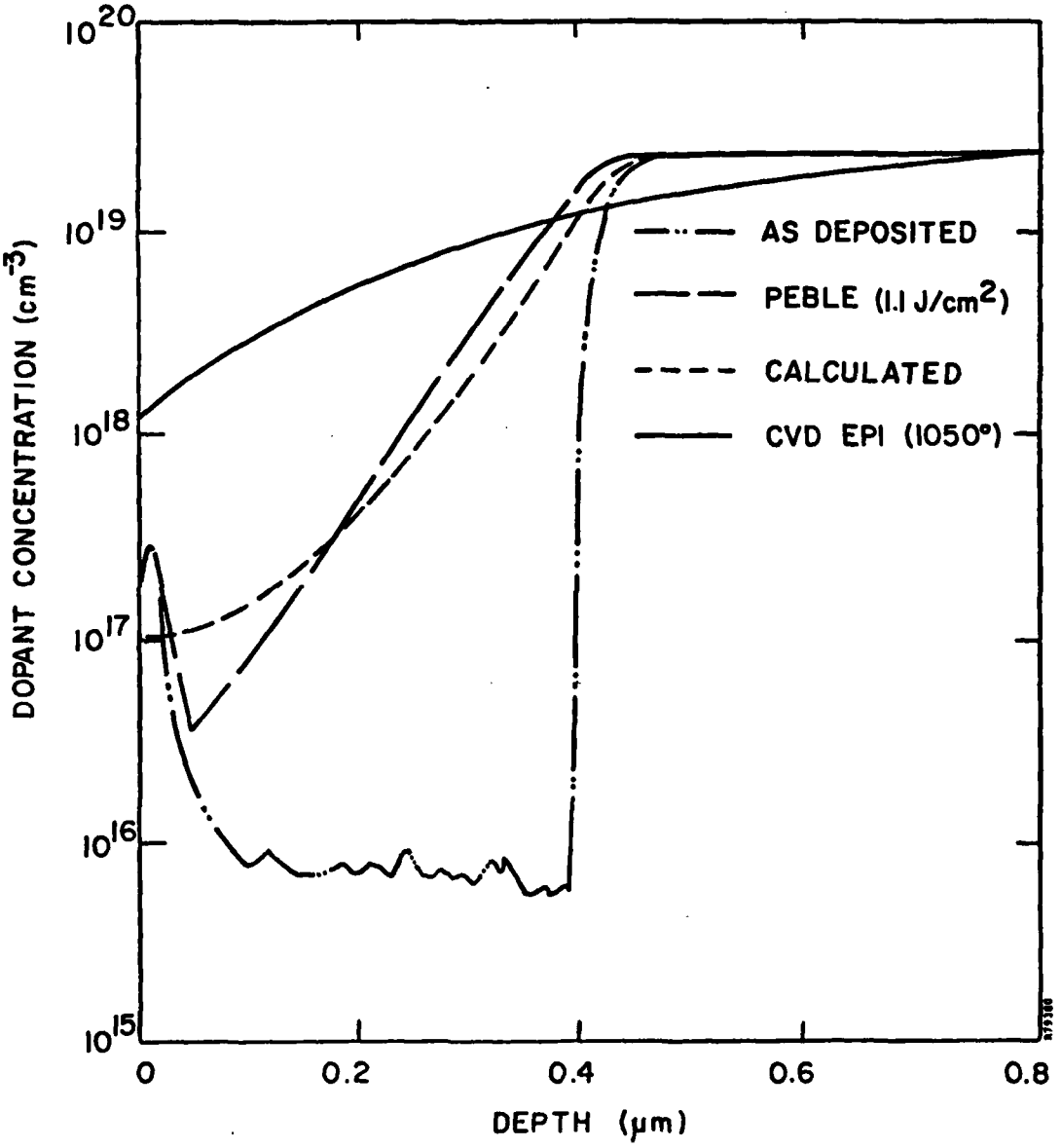
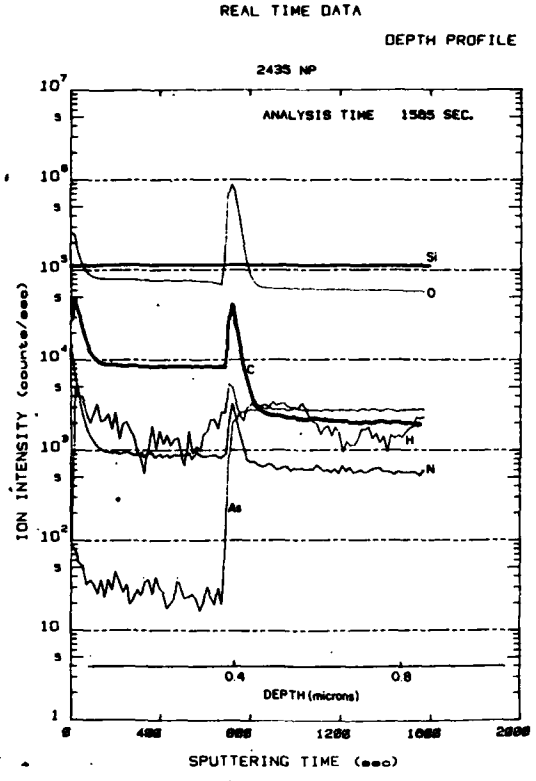


FIGURE 2-3. SIMS profile of arsenic in as-deposited LPCVD films, in the same sample after PEBLE, and in conventional epitaxial material compared to a theoretical calculation for dopant redistribution for the thermal model in Figure 2-1.



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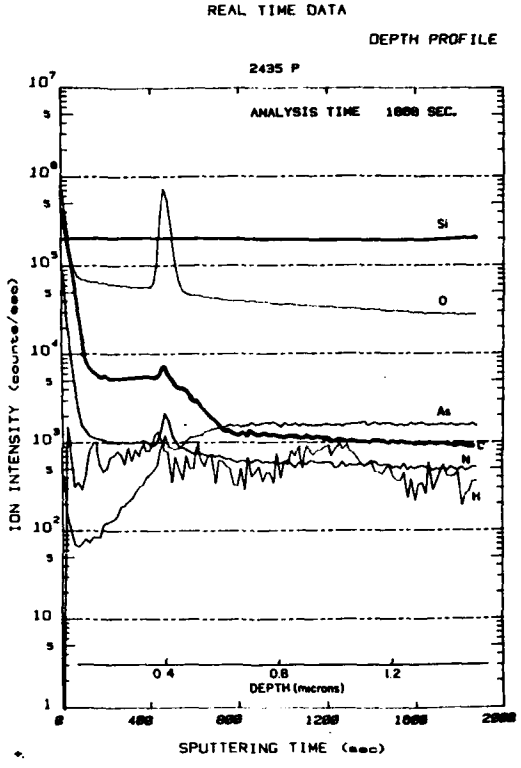


After

FIGURE 2-4. SIMS profile of As, C, H, N, and O before and after pulsing 0.4 μm LPCVD polycrystalline silicon films, showing the increased concentration of impurities at the original substrate interface. Note measurement induced broadening of 15Å interface and lack of oxygen diffusion.

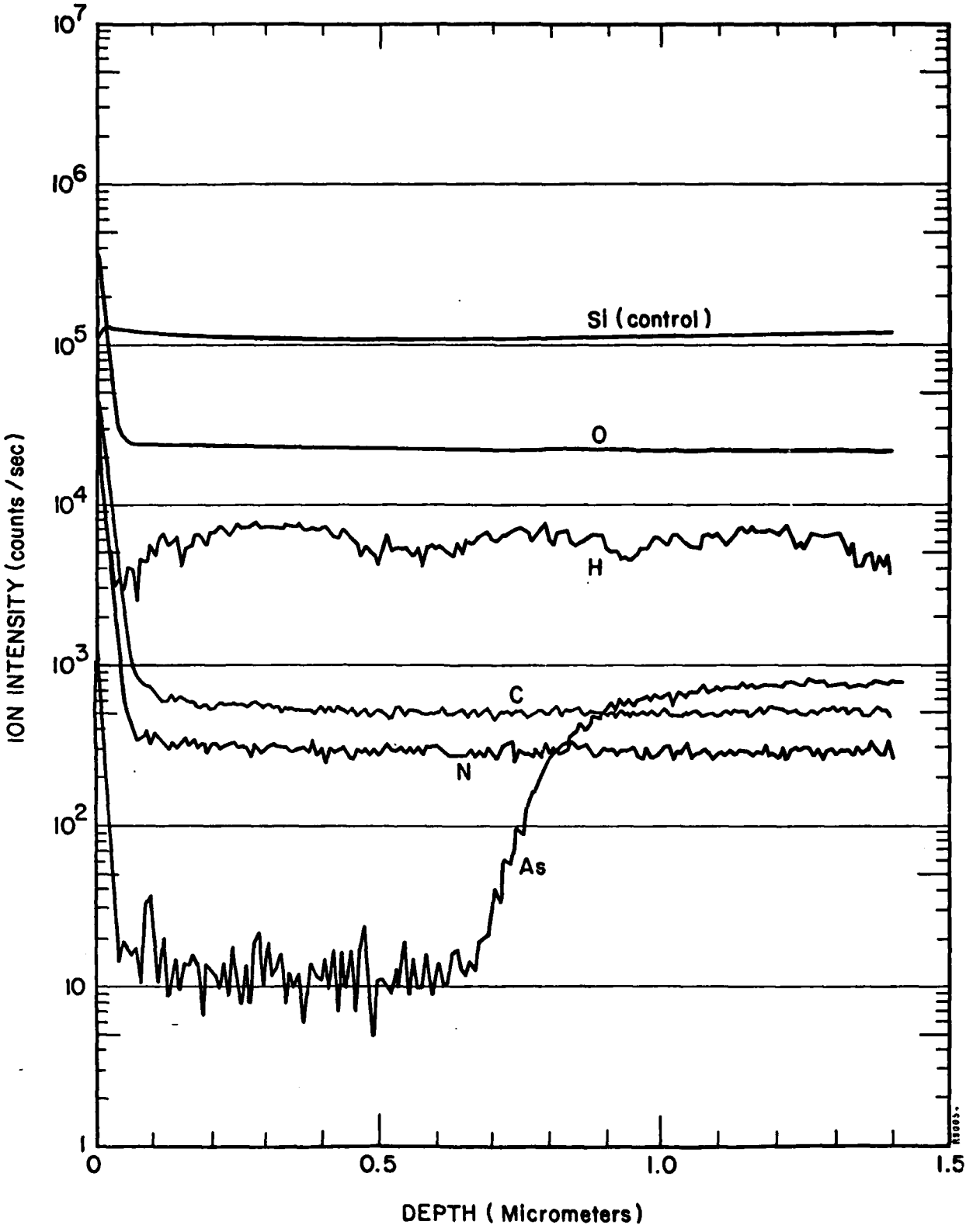


FIGURE 2-5. SIMS profile of C, H, N, O, and As in 0.5 micrometer CVD epitaxial film deposited on a 0.003 Ω-cm substrate from $SiCl_4$ at 1150°C. Note level of contaminants in substrate and film is identical, which is not observed in Figure 2-4.

2.3.2 LPCVD from Hewlett Packard

The goal of this second experiment with LPCVD films was to compare amorphous and polycrystalline films for PEBLE. The original test matrix is shown in Table 2-1. Wafers without junctions and wafers with ion implanted, furnace or pulse annealed junctions were submitted for LPCVD at 625°C (polycrystalline) and 550°C (amorphous) deposits. In addition, one wafer which was ion implanted only and one other wafer which was implanted and furnace annealed only were kept for controls.

The substrates used were 3-inch o.d. FZ (float zone) silicon wafers. They were p-type (boron doped) 1 ohm-cm with a polished surface. The implant was 25 keV arsenic at $1 \times 10^{16}/cm^2$ dose. The furnace anneal was at 550°C for 1 hour and then 950°C for 15 minutes. The pulse anneal was at 1 J/cm^2 (melting) and uniform[5]. All wafers were cleaned, oxide stripped, and put into the reactor (in N_2 gas flow) at 500°C to minimize oxide growth. The residual oxide was not etched off in the reactor. The wafers were heated to the deposition temperature, either 625°C or 550°C, and silane was added at 0.25 torr. Approximately 300 nanometers was deposited. At Spire Corporation, a back contact of Ti-Pd-Ag was evaporated onto these samples for uniform pulse treatment.

The film deposited at the lower temperature, 550°C, was supposed to be an amorphous layer. Visually, it was very smooth and appeared to be a slightly different color than the polycrystalline films deposited at 625°C. This was confirmed by ellipsometry. However, RHEED analysis showed a polycrystalline surface. Further, the diffraction pattern contained unidentified lines. There appeared to be no difference in the deposits on implanted and pulse annealed, or furnace annealed, or unimplanted wafers. Analysis by SIMS, Figure 2-6, showed that the film was contaminated with hydrogen, nitrogen, and carbon compared to the deposits from Applied Materials (Figure 2-4). This contamination explained the diffraction lines and later results.

2.3.3 CVD from Microwave Associates, Inc.

Noting the possible contamination of silicon films deposited at very low temperatures in an LPCVD reactor, a comparison was made with low temperature deposition in an infrared heated reactor from Microwave Associates, Inc. The substrates and film parameters given were identical to those furnished to Applied Materials. The deposits appeared to be similar.

The substrates were 2-inch o.d. (111) silicon wafers doped with arsenic to 0.003 ohm-cm. The backs of the wafers were not epi-sealed. They were etched in buffered HF

TABLE 2-1. Experimental matrix for studying pulse epitaxy over a buried junction layer formed by pulse annealing. These six types of samples were pulsed for epitaxial regrowth of the film and analyzed for crystal structure, dopant profile, and impurities.

Substrate Preparation	LPCVD Film
Not implanted	Amorphous
Implant Pulse Anneal	Polycrystalline
Implant Furnace Anneal	

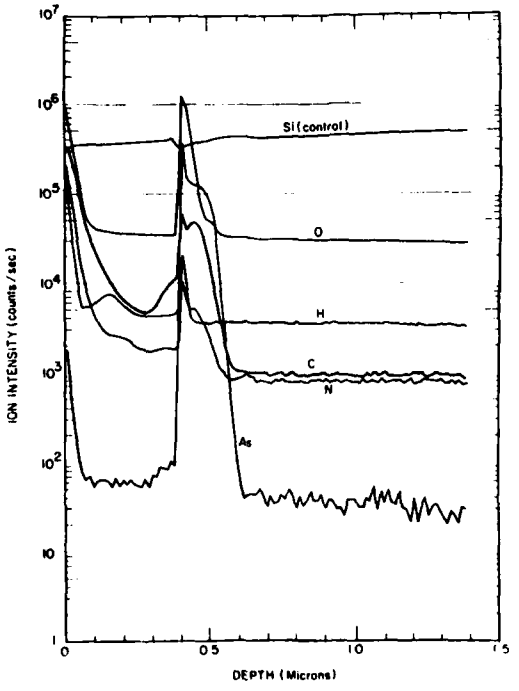


FIGURE 2-6. SIMS profile of As, C, H, N, and O in a CZ p-type wafer implanted with $1 \times 10^{16}/cm^2$ 25 keV As, pulse annealed, then covered with an amorphous 0.4 μm LPCVD film deposited at 550°C. Note excess hydrogen in film compared to Figure 2-4.

solution before insertion into the reactor, but were not etched in situ with HCl. The film was deposited from silane in H_2 carrier gas at 650°C. The final film thickness was 400 nanometers. Doping was $10^{15}/cm^3$ as measured by a four point probe.

The films were uniform, and smooth from optical observations. Diffraction (RHEED) showed a polycrystalline structure of pure silicon. These patterns were very similar to those obtained from LPCVD films.

2.3.4 CVD Films from Spire

This section briefly reviews those films deposited by CVD at Spire during the first 6 months of this program as a comparison to LPCVD results. The significant difference is the use of higher temperatures. The reactors at Spire cannot be reliably operated below 840°C.

The substrates used were identical, (111) arsenic doped silicon of 0.003 ohm-cm. These wafers were bright etched on the back and polished on the front. A few similar wafers of (100) orientation were used for comparison. The wafers were cleaned and etched in HF solution just before insertion into the reactor. On some wafers the remaining oxide was etched off at 1200°C before deposition. This step did not seem to affect further results. Films were deposited from silane at 840°C at about 50 nm/s. Unintentionally, some dopant was added to the gas bringing the arsenic concentration up to $10^{17}/cm^3$ in the film.

The films deposited at Spire Corporation were very sensitive to handling and were not, on average, as smooth and uniform upon visual examination as the LPCVD results. Some deposits were textured and showed growth of pyramid crystallites from the surface about 0.5 micrometer high. Analysis by RHEED and SEM showed an oriented polycrystalline structure, with large (0.5 micrometer) grains. No contaminants were detected in these films.

2.4 ANALYSIS OF PULSED EPITAXIAL REGROWTH

Samples of all deposited films were heated by a pulsed electron beam. At high fluence (energy/unit area) a change in the structure of the film was observed. Most films showed epitaxial regrowth. This result was reproducible. This phenomenon can be modeled as a molten film showing liquid phase epitaxial growth when cooled by thermal conduction through the crystal substrate. Dopant concentration profiles agree with this model.

2.4.1 Pulsing Conditions

All experiments were done on the SPI-PULSE^{TM} 5000 electron beam processor. The electron beam diode consists of a cold cathode and mesh anode. The diode voltage and current as a function of time is shown in Figure 2-7, along with the interpreted electron energy spectrum. The electron beam pulse ends when the voltage reaches zero. The rising current causes the beam to self-focus at the sample position. This focusing results in nonnormal incidence of the electrons upon the sample, heating the surface more strongly. This is shown in Figure 2-8, a calculated temperature time profile[5].

2.4.2 Experimental Results on LPCVD

Pre- and postpulse analysis of LPCVD films from Applied Materials for structure and dopant distribution are shown in Figures 2-2 through 2-4. This data implies that the surface was melted by the electron beam pulse and regrew with an epitaxial structure upon solidification.

Electron diffraction patterns (Figure 2-2b) from RHEED[6] analysis are characteristic of single crystals with long range order. No twinning is observed. This was from a sample irradiated at 1.1 J/cm^2. The experiment was repeated with identical results. At lower fluence (0.9 J/cm^2) there was no change in the diffraction pattern (Figures 2-2a and b), implying either that the film did not melt or that the depth of melt did not extend from the surface to the substrate.

The dopant profile was determined by SIMS analysis because it could not be determined by electrical measurements in the initial polycrystalline material. As shown in Figure 2-3 the concentration of arsenic at the original substrate film interface falls off more rapidly from PEBLE than from conventional CVD. Also, the shape of the concentration-depth profile is not characteristic of solid phase diffusion or autodoping. It can be matched only by a melt model. The carrier distribution was also measured by C-V analysis (Figure 2-9). This shows a sharper boundary than SIMS; however, not all of the dopant may be substitutional. These measurements, on the lower doped Sb substrates, imply that the motion of dopants with low segregation coefficents is identical.

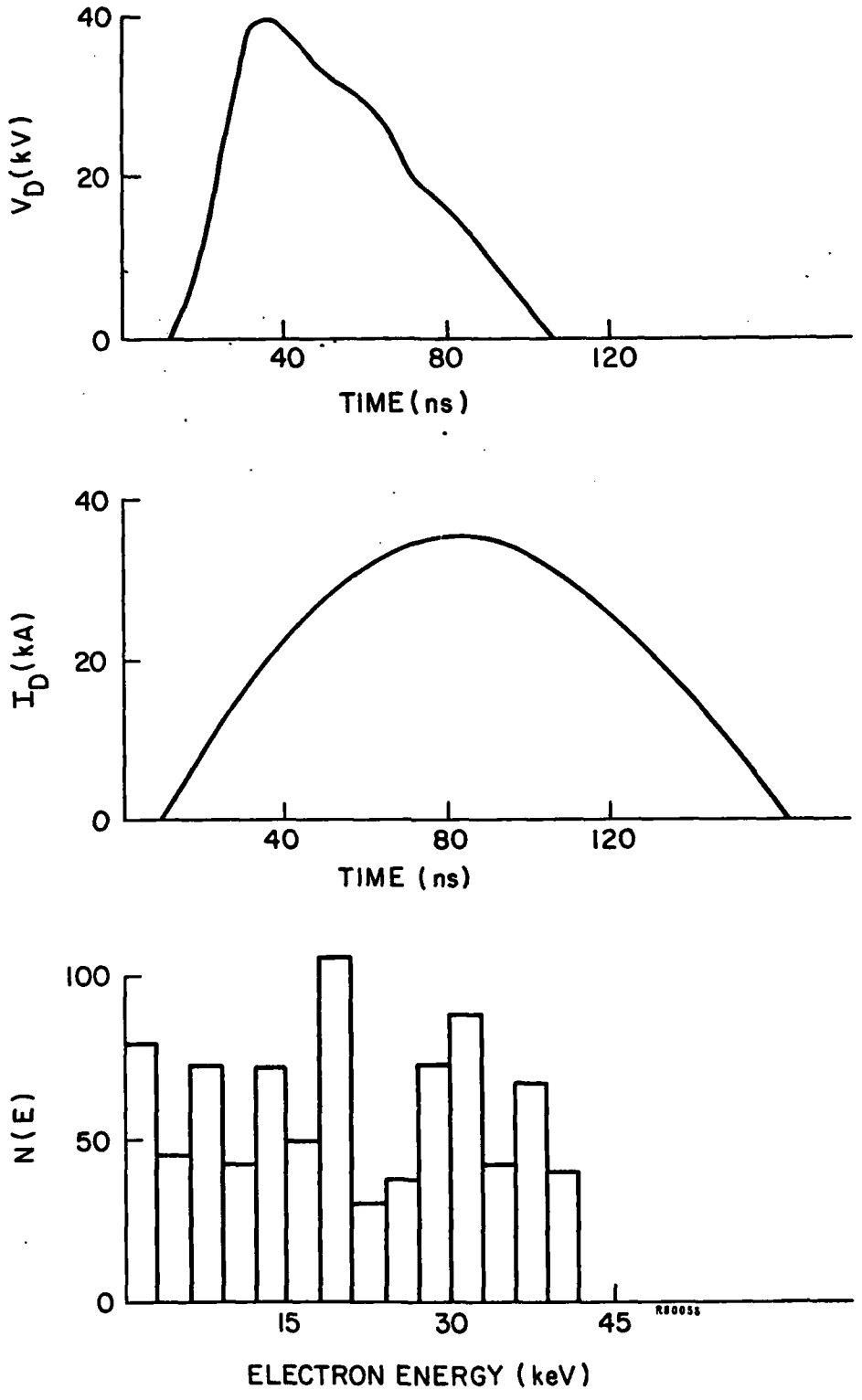


FIGURE 2-7. Electron beam machine diode voltage and current traces as a function of time and interpreted electron energy spectrum for the beam used in epitaxial regrowth experiments.

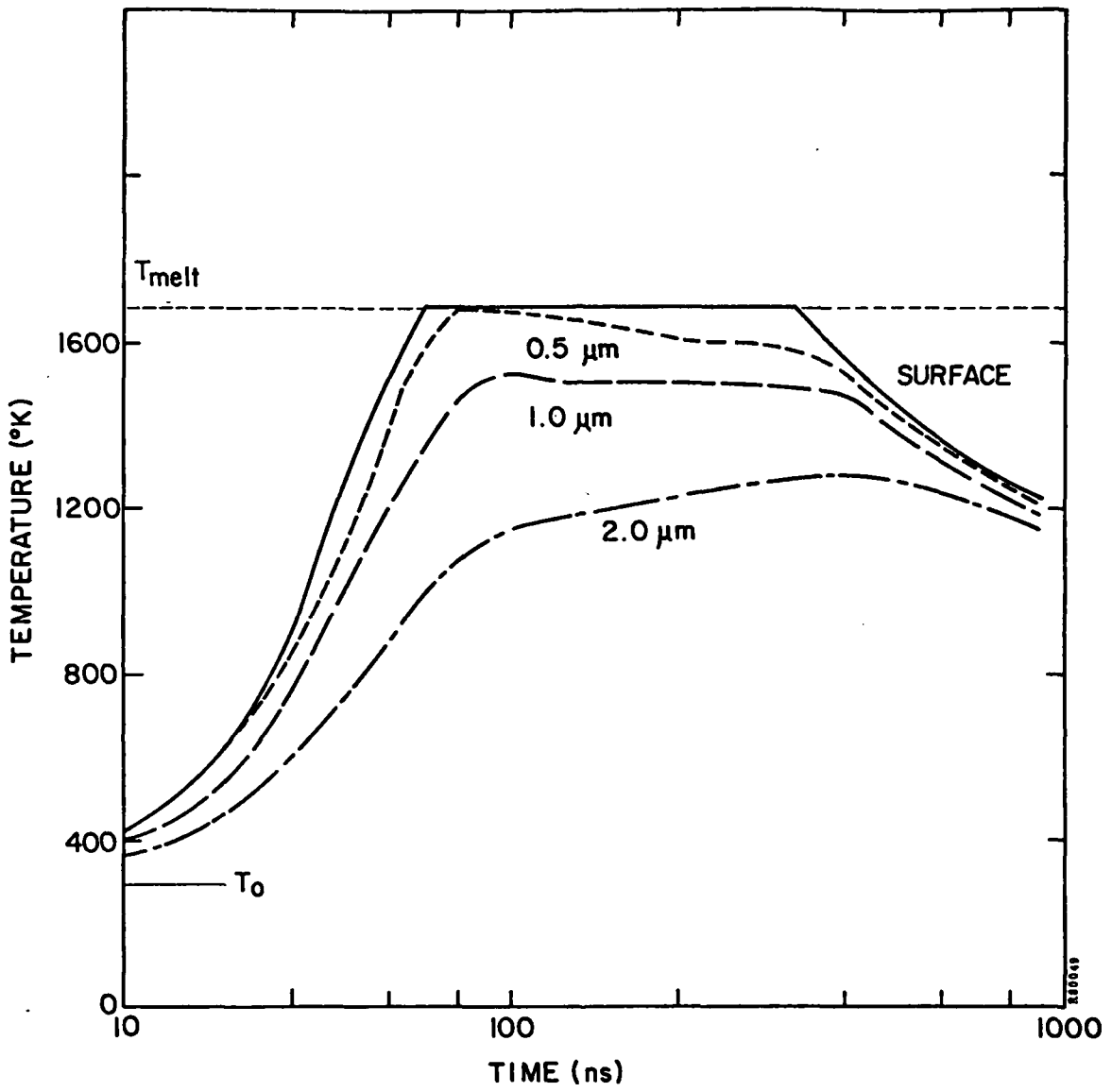


FIGURE 2-8. Temperature as a function of time for different depths in silicon irradiated by a pulsed electron beam at 1.2 J/cm^2 with an 80-ns pulse width. Note that the maximum melt depth is 0.5 μm in this case.

Figure 2-4 shows the effect of melting upon the distribution of contaminants at the original substrate surface, which was not etched in the reactor before deposition. Arsenic and carbon have moved away from this interface while the nitrogen and oxygen profiles remain virtually unchanged. There also appears to be a slight increase in arsenic concentration at the interface. This result is contrary to the model reported in the literature[8,9] for laser melting and regrowth, where it was believed that the oxygen originally at the interface would diffuse throughout the bulk of the silicon to the solid soluability limit. The fact that the LPCVD film did show epitaxial regrowth after melting implies either that (1) the thin oxide layer (if continuous) did not inhibit crystal growth or that (2) the oxide film is not continuous, a condition which allows the crystal structure to grow through this layer and around the impurity. Further analysis is required to show which explanation is correct.

2.4.3 Analytical Model for Pulsed Electron Beam Liquid Epitaxy

The electron beam penetrates and heats substantially a region as thick as 0.5 micrometer (Figure 2-8). This observation implies that until the surface melts, there is a region at the melt temperature which has not received the heat of fusion. After initiation of melting at the surface, the solid-liquid interface moves inward towards the substrate very rapidly, over 0.5 micrometer in 10 nanoseconds. Thus, it is possible to assume nearly instantaneous melting of the polycrystalline layer, a condition different from laser melting, where maximum energy absorption is confined to the surface ($\sim$100A) at high temperatures and the melt depth will reach a maximum <u>after</u> the laser pulse.

For the calculation in Figure 2-3, the film plus a 10 percent greater depth is assumed to be melted at t=0. There has not yet been a change in dopant distribution. The molten silicon cools by conduction to the substrate. The liquid-solid interface is assumed to move at a constant speed of 1 m/s towards the surface[10]. In the liquid, the diffusion coefficient of the dopant, arsenic, is assumed to be 3.0×10^{-4} cm^2/s[11], while in the solid, diffusion is neglected because the coefficient is about 9 to 10 orders of magnitude smaller. The profile shown was calculated by solving the diffusion equation with a finite element numerical code. The results are extremely close to the actual profile, while a straight diffusion calculation[12] would give an erfc curve which would not match. This is taken as strong indirect evidence for melt.

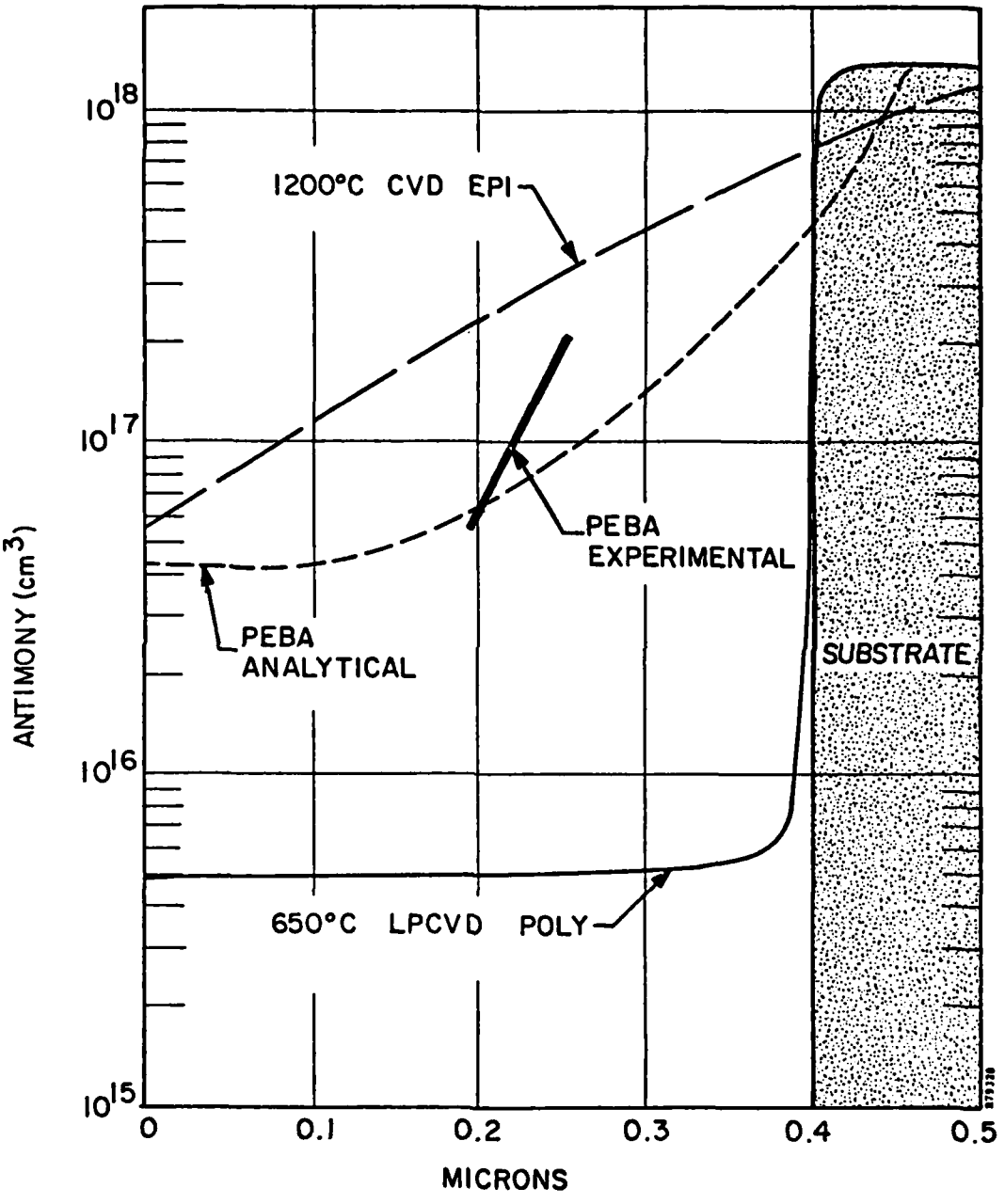


FIGURE 2-9. Antimony profiles in silicon films comparing 1200°C CVD epitaxy, 625°C LPCVD poly, and the same poly film after pulsing (C-V profile). Note the analytical calculation based on the model in Figure 2-1 and the similarities to Figure 2-3.

2.4.4 Additional Pulsed Epitaxy Experiments

In contrast to the epitaxial growth described after pulsing so far, some films at the same fluence (1.1 J/cm^2) showed no regrowth and only polycrystalline phases. The material from Hewlett Packard, after pulsing, showed a distinct change in color, which was initially believed to be an amorphous to epitaxial change. Analysis by RHEED, however, showed that the material remained polycrystalline after pulsing with no change in the unidentified diffraction lines. Similar results were obtained with the low temperature CVD films furnished by Microwave Associates; however, there was no change in optical properties after pulsing these films.

The interpretation of the data is that a higher fluence is possibly required for epitaxial regrowth of these samples. Alternately, a contaminant may have prevented good crystal regrowth, or the impurity could have segregrated to the surface through the zone refining mechanism[13] and ruined the crystal structure in the top 10 nanometers seen by the electron beam at a high angle of incidence. The change in color on some LPCVD samples would imply some change in structure, possibly an increase in grain size or a change in dopant concentration. In either case, more analysis needs to be done.

2.4.5 Experiments in Progress

The first objective in task 2 of this program is to show how the crystal structure of the deposited film, particularly the change between polycrystalline and amorphous material, influences the pulse processing. It is believed that better control of the melt depth and a lowering of the threshold fluence would result when pulsing amorphitized surfaces. To this end, some samples of poly films were implanted with silicon at 25 keV to a high dose of $5 \times 10^{15}/cm^2$. This should be sufficient to turn the surface amorphous[14]. These films will be examined and compared to similar, nonimplanted pulsed results.

SECTION 3
PULSE ANNEALING ION IMPLANTATION DAMAGE

3.1 OBJECTIVE OF TASK 3, PULSE ANNEALING

The objective of this task is to form junctions in silicon by ion implantation and low temperature, directed energy annealing processes. A given restriction is to minimize the redistribution of the implanted dopant either laterally or as a function of depth during the pulse processing. This requirement is a variation on the pulsed electron beam annealing (PEBA) process already demonstrated[5] which melts the surface, leading to dopant redistribution, and anneals by liquid phase epitaxial regrowth of the crystal.

A pulsed, nonmelting technique is required to minimize the wafer temperature and dopant diffusion. This type of annealing has been demonstrated using a CW ion laser[15], but with an unacceptably slow process throughput (typically one 3-inch wafer per hour). The technology to be demonstrated here is easily capable of a throughput of one 3-inch wafer per minute, typical of production lines today.

3.2 ANALYTICAL MODEL OF ANNEALING MECHANISM

Annealing of ion implantation damage is perceived as a two step process.[16] As a first step, for heavy damage, the structure of the crystal surface must be restored by epitaxial crystal growth from the substrate towards the surface. The second step, which is all that is required for lightly damaged regions, removes localized defects in an ordered crystal structure and activates the implanted dopant. It is the second step which requires high temperatures, but the first step that requires the most time.

To meet the requirements of an optimized two step anneal with pulsed processing, two approaches were devised. The first approach used only pulsed heating, with multiple pulses required to meet the time requirement for crystal regrowth. The second approach used a low temperature furnace (550^{o}C) for lattice regrowth and only one pulse to replace the high temperature step. It is noted that the two step process discussed can be accomplished in one single, high temperature heating cycle in a furnace where the wafer temperature is ramped up and down slowly. For this process, the typical minimum cycle time is one-half hour.[17]

3.2.1 Solid Phase Anneal by Multiple Pulses

The regrowth rate for annealing ion implantation damage in silicon is shown in Figure 3-1 as a function of temperature.[18] This data was gathered from shallow junction implants where the heavily damaged (amorphous) surface region was restricted to 50 nanometers (the junction was deeper). This curve agrees with data from sweeping CW lasers or d.c. electron beams with an equivalent pulse length of 50 microseconds to 10 milliseconds. If it is assumed that the important variable is the total time at high temperature, and that the heating cycle is not as significant for fast pulses, then a sequence of very short (0.1 microsecond) pulses can be used to anneal implantation damage in the solid phase. From the data given in Figure 3-1, a minimum total time of 50 microseconds can be estimated. For the pulsed electron beam at Spire, with a total pulse width of 0.1 microsecond, the surface is expected to remain at high temperatures approximately 0.5 microsecond (Figure 2-8). This implies that approximately 100 pulses are required for complete annealing.

This process has two advantages over the competing C-W lasers and electron beams. The first is throughput. Demonstrated throughput for laser processing (not pulsed) is less than one wafer per hour[15] with one 40 to 100 micrometer line width annealed at a rate of 1 - 10 cm/s. A d.c. electron beam has somewhat better throughput, as fast as six 4-inch wafers/hour, because the total power and beam diameter can be larger. The pulsed electron beam has a repetition rate as high as 10 pps, so that large wafers can easily be processed at a rate of one per minute. The second advantage is that the laser and d.c. electron beam techniques have used heated wafers (up to 350°C) for the optimum results, and have had high temperatures in the bulk of the material for longer periods of time. Pulsed beam techniques use room temperature processing only and keep the temperature lower, on average, in the substrate.

3.2.2 Furnace-Pulse Combinations

Typical thermal cycles for annealing ion implantation damage in silicon used in industry today are either one step[17], where the wafer is slowly ramped up to a high temperature (900 - 1000°C) and then ramped back down, or two steps[16], where the wafer is held for an extended time at an intermediate temperature (550°C) then for a short time (10 - 15 minutes) at high temperatures. For a low temperature processing technique, only the short high temperature step need be replaced.

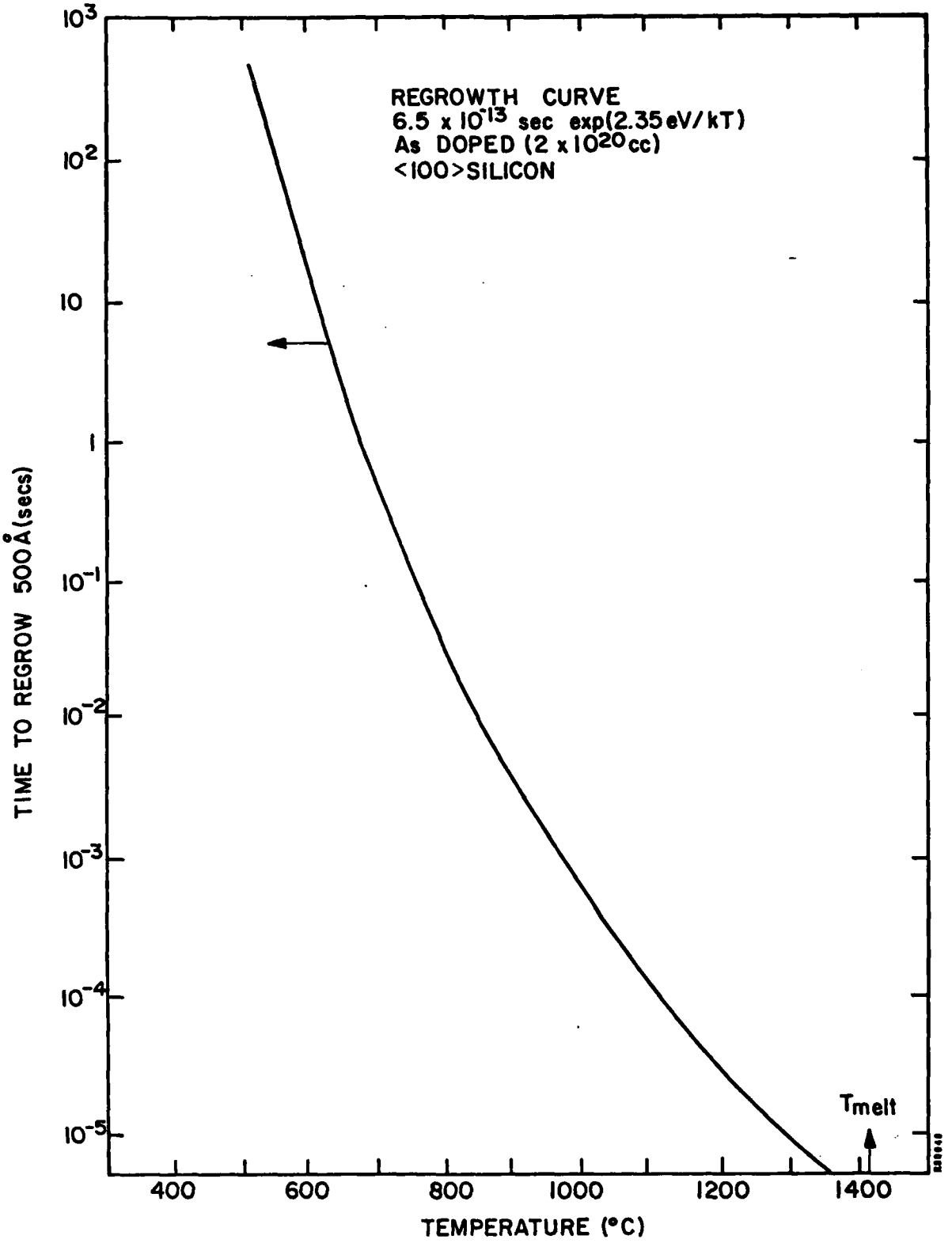


FIGURE 3-1. The time to epitaxially regrow 500Å of amorphous (ion implanted) silicon as a function of substrate temperature, from Reference 18.

The justification for the short high temperature treatment is the improvement in the amount of implanted dopant which becomes substitutional. Analysis has shown that the crystal lattice is largely restored after a long time low temperature anneal. It is inferred that the defects removed from the lattice, and the change of dopant from interstitial to substitutional site at high temperatures, involves changes in short range order in the crystal. The time required for this change is much less than the time required to regrow the lattice structure in heavily damaged material, and will not be a limiting factor. A short pulse should be able to replace this second furnace step.

3.3 PULSED ELECTRON BEAM ANNEALING EXPERIMENTS

3.3.1 Multipulse Solid Phase Anneal

This experiment was reported previously[5]. A pulsed electron beam was developed which could be repeatably impinged upon a silicon sample without melting it. Wafers were prepared for this test with a very shallow junction to minimize the number of pulses required for regrowth of the surface. The implants were high dose to create an amorphous surface ($2.5 \times 10^{15}/cm^2$ 10 keV phosphorus, or $1 \times 10^{16}/cm^2$ 100 keV arsenic). After 100 pulses the amorphous surface turned to polycrystalline silicon. There was no movement of the dopant, implying no melting. A piece of this material was submitted to the California Institute of Technology for analysis by RBS (Rutherford backscattering) as part of a cooperative industry-university program. Results are not available yet.

The change in surface morphology, from amorphous silicon to crystalline silicon, prior to complete regrowth of the crystal structure implies that the thermal cycling of the sample during the anneal process is important, not just the total time at high temperature. It is not possible to anneal implant damage from a randomly oriented polycrystalline surface without melting. This observation implies that a change in the heating cycle must be made, but no further work has been done.

3.3.2 Single Pulse Liquid Phase Anneal

Most of the pulse anneal development has been based upon a melting model. The implanted region is melted and regrows by liquid phase epitaxy, similar to Figure 2-1. The results of this type of anneal are shown in Table 3-1 for two experiments.[5,19] At this fluence (0.9 J/cm^2) an amorphous surface on silicon will melt, but a nearly crystalline surface will not[5]. Thus, high dose implants (10^{15} - $10^{16}/cm^2$) are annealed

TABLE 3-1. Sheet resistance for arsenic implanted (100) p-type silicon comparing pulse electron beam liquid phase anneal and furnace anneal.

Implant Dose (cm^{-2})	Implant Energy (keV)	Sheet Resistance	
		Pulse Anneal[a] (ohms/□)	Furnace Anneal (ohms/□)
10^{13}	25	1200	388 [b]
10^{14}	25	252	168 [b]
10^{15}	25	107	148 [b]
10^{14}	100	813	388 [c]
10^{15}	100	102	84.5 [c]
10^{16}	100	21.6	28.2 [c]

(a) Pulse at Spire at 0.9 J/cm^2.

(b) 2 hours at 550°C, 1 hour at 850°C Spire.

(c) 1-1/2 hours at 550°C, 1-1/2 hours at 600°C, 10 minutes at 1000°C TRW.

when the surface is heavily damaged, but low dose, less damaging implants are not. Note that 100 keV arsenic ions will not create an amorphous surface at $10^{14}/cm^2$ implant dose, while 25 keV As ions will create much greater surface damage (nearly amorphous) at the same dose. This explains the differences between pulse and furnace anneals in Table 3-1 for this implant dose.

The sheet resistance for annealed, boron implanted wafers is given in Table 3-2[19]. These implants at 100 keV do not create an amorphous surface layer, and it is believed that the surface was not melted. The sheet resistance after only one pulse is high, and the surface incompletely annealed. After pulsing, the wafers were given the same thermal cycling as those samples annealed in a furnace alone. The sheet resistance after this treatment is identical to the furnace annealed samples. This experiment was performed for both (111) and (100) orientations with no significant difference in results.

TABLE 3-2. Sheet resistivities for 100 keV boron implants into silicon comparing the effect of various thermal cycles after pulse processing.

		Sheet Resistance (ohm/□)					
				550°C for 1.5 h + 600°C for 1.5 h		550°C + 600°C + 1000°C for 10 min	
Implant Dose	Orientation	After PEBA	Not Pulsed	Pulsed	N.P.[a]	Pulsed	N.P.
10^{14}	(100)	897	10,000	1000	1340	545	547
10^{14}	(111)	1098	10,000	1010	1480	543	543
10^{15}	(100)	218	10,000	323	842	92.8	94.1
10^{15}	(111)	547	10,000	324	811	93.8	92.2
10^{16}	(100)	707	10,000	95.7	316	27.7	21.4
10^{16}	(111)	288	10,000	24.6	736	22.5	22.3

[a] N.P. = Not pulsed.

3.3.3 Furnace-Pulse Combination

The early experiment[19] showed some improvement in sheet resistance after pulsing for low temperature thermal treatment. As proposed, the pulse should follow the low temperature anneal step, and this experiment was repeated. The new results are shown in Table 3-3. The implant energy was changed to 25 keV, and the thermal cycles changed to match the equipment usage at Spire Corporation. N-type (phosphorus) doped substrates, 4 to 20 ohm-cm (111), were implanted with 10^{13}, 10^{14}, and $10^{15}/cm^2$. They were annealed by varying thermal treatments:

a) 550°C for 1 hour
b) 550°C for 1 hour, plus 950°C for 1 hour
c) 550°C for 1 hour, plus 950°C for 15 minutes
d) 550°C for 1 hour, plus pulse at 1.0 J/cm^2
e) 550°C for 1 hour, plus pulse at 1.25 J/cm^2
f) Pulse at 1.0 J/cm^2 only

TABLE 3-3. Sheet resistance (ohms/□) of 25 keV boron implants into 8-20 ohm-cm n-type silicon showing effects of pulse annealing after low temperature heating.

Annealing Cycle	Implant Dose (ions/cm^2)		
	10^{13}	10^{14}	10^{15}
550°C 1 h	10,000 Ω/□	2800 Ω/□	1600 Ω/□
550°C 1 h + 950°C 1 h	—	531	99
550°C 1 h + 950°C 15 min	1900-3700	640	110
550°C 1 h + pulse @ 1 J/cm^2	2940	960	140
550°C + pulse @ 1.25 J/cm^2	2140	720	153
Pulse @ 1 J/cm^2	3600	910	140

Higher fluence pulses caused damage by excess thermal shock; lower fluence pulses yielded less than optimum results. All furnace heating was in a dry nitrogen atmosphere.

This experiment, compared to the results in Table 3-2, showed that a low temperature furnace cycle before pulsing was much more effective than a similar cycle after pulsing. It also showed that sheet resistance values comparable to high temperature furnace cycles can be achieved by this technique. Also, pulsing after a low temperature thermal treatment was much more effective in annealing than just that thermal treatment alone, or using longer cycles at low temperatures.

A second set of samples with an implanted dose of 10^{14}/cm^2 (25 keV boron) was prepared to determine the dopant depth profile using secondary ion mass spectroscopy (SIMS). The surface of the samples was sputtered at a constant rate (about 2.5 Å/s) using an oxygen beam. The results are shown in Figure 3-2. The low temperature (550°C) thermal treatment led to a very small displacement of the implanted dopant profile, which is attributed to diffusion enhanced by radiation damage. The motion of the dopant during the pulse anneal is comparable to the diffusion at high temperatures

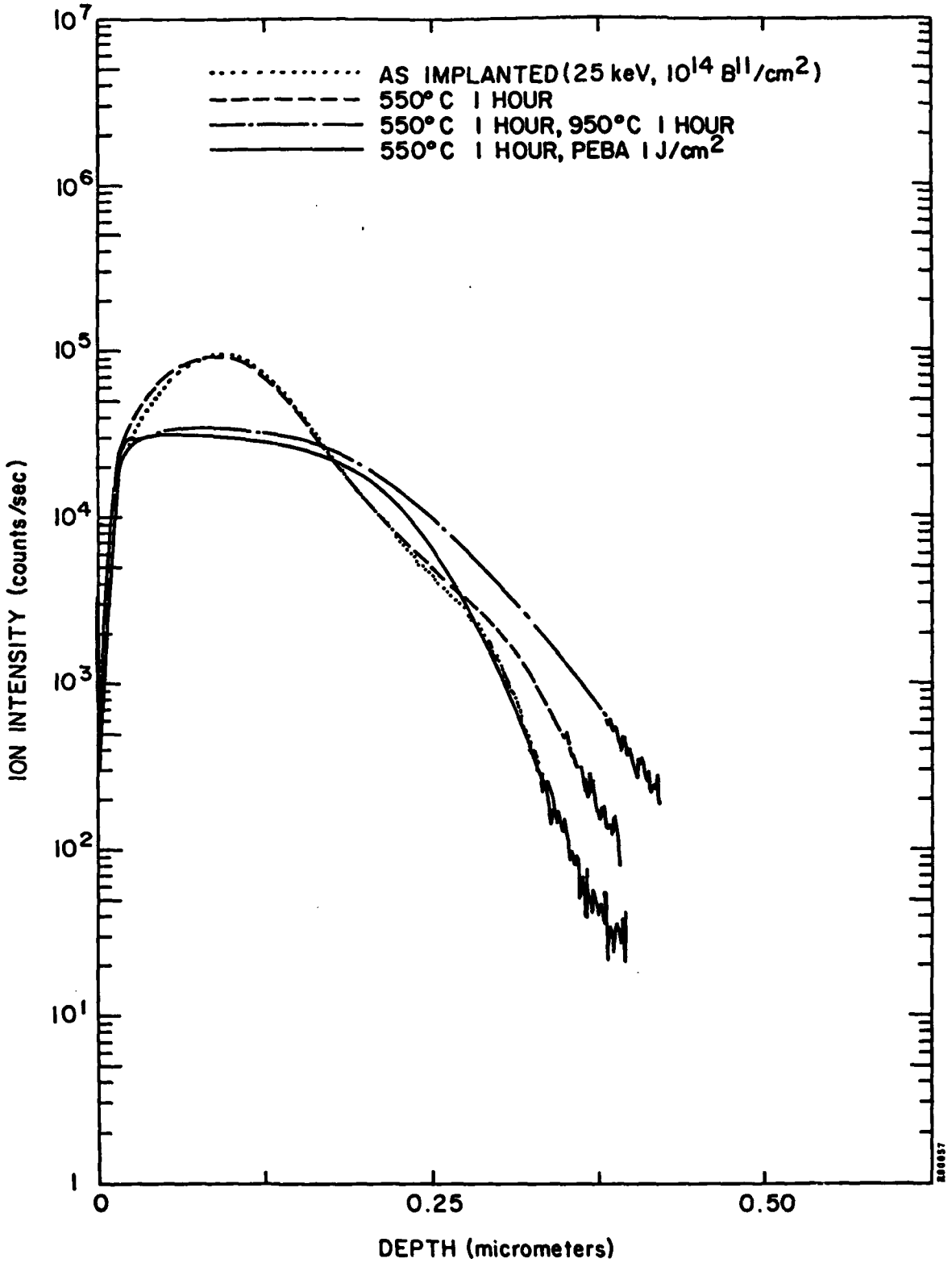


FIGURE 3-2. SIMS profiles of boron implanted into silicon showing relative motion of the dopant for different anneal cycles.

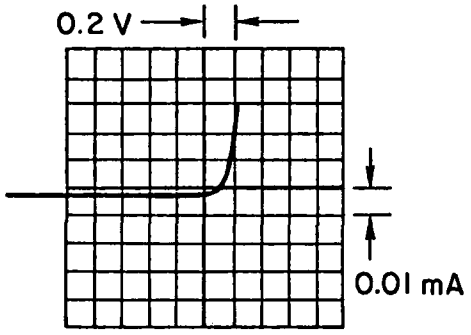
temperatures. The difference in the shape of these curves could be attributed to the motion of dopant in a melt where the time the liquid exists is greatest at the surface and decreases with depth (see Section 2).

This is the first evidence that the pulse was possibly melting the crystal silicon. If true, it is not clear why the pulse alone could not anneal the implant damage. The results could be explained if the crystal silicon were not melted deep enough to anneal out all damage from the boron implants. To answer this question, mesa etched diodes were formed on these samples to determine electrical characteristics and search for deep lying defects.

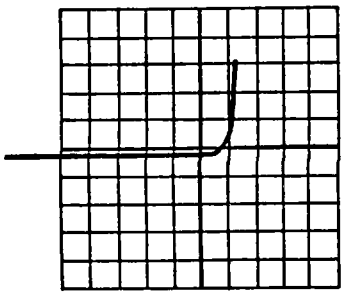
3.4 TEST STRUCTURES

Work on task 4, Device Fabrication, was initiated. Mesa diodes were etched in the samples listed in Table 3-3. After the initial annealing treatment listed, and after measuring the sheet resistance, a back contact and front contacts consisting of 20-mil dots were evaporated onto the substrate and sintered at 400°C for 5 minutes. The contact metallization was TiPdAg (1 micrometer). The back contact was covered by tape and the front dots covered by 100-mil circles of photoresist during etching in a solution of nitric acid, acetic acid and hydrofluoric acid (5-3-3). The properties of these diodes were measured at several points on each wafer with uniform results.

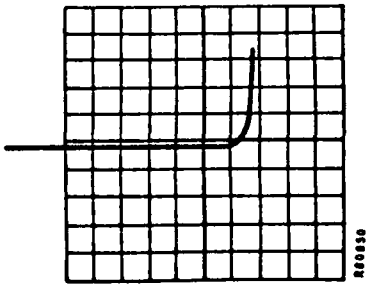
The I-V characteristics from the wafers with $10^{15}/cm^2$ implants of boron are shown in Figure 3-3. The pulse processed devices that had received a 1 hour 550°C preanneal compared favorably with the devices that had the two step high temperature anneal. They showed good characteristics with low leakage current, but there was evidence of process induced point defects[20] which were reduced by a 5-minute 500°C postanneal (compare Figures 3-3a and 3-3b). The postanneal time and temperature in this experiment was limited by the metallization on the wafer. Higher temperatures for longer periods will be tried on devices prior to metallization to investigate this annealing effect further. Future measurements will include capacitance-voltage measurements of pulse processed diodes, using a Miller feedback profile plotter to study possible process induced carrier removal effects in the substrate, and to optimize the postannealing for reducing both the carrier removal effects and the point defects.



a) 550°C 1 HOUR
PEBA 1 J/cm^2



b) 550°C 1 HOUR
PEBA 1 J/cm^2
500°C 5 MIN



c) 550°C 1 HOUR
950°C 15 MIN

FIGURE 3-3. I-V curves for ion-implanted (boron, 25 keV, 10^{15}/cm^2) mesa diodes comparing the effect of different anneal schedules. Note that (b) would be improved if post-pulse anneal treatment were longer (Table 3-2).

3.5 PULSE ANNEALING PROCESS VARIABLES

3.5.1 Variation with Ion, Energy, and Dose

The fluence required to melt the surface of a silicon wafer (to 0.5 micrometer) varies with amorphous and crystalline material. The implant dose required to create a very heavily damaged, amorphous surface in silicon varies with the ion mass and energy. This implies that the optimum fluence for pulse annealing with melting will vary with the implant parameters. Without melting, the principal variation is depth of heating required, which also varies with implant parameters. For example, this work implies that boron implants, which cause damage deeper than arsenic implants, require higher fluence (1.25 J/cm^2 versus 1.0 J/cm^2) for optimum annealing. This fluence will have to be found by experiment and a matrix is planned.

There is a limit, now unknown, to the maximum ion energy which can be pulse annealed. As the depth of damage increases, the fluence required increases past the point of surface melt, and eventually reaches a damage threshold where thermal stress cracks the surface. Since VLSI technology requires thinner layers, this limit should not be a problem for this program.

3.5.2 Variation with Surface Oxides

Experiments to date have only used samples with the entire surface bare and implanted. Such samples have limited application to devices, since it is expected that ion implantation damage annealing will occur when there are patterned oxides on the wafer surface and possibly even more complex multiple-layered geometries. At high fluence, thin SiO_x layers on silicon show characteristic wave patterns after pulsing.[21] These patterns have height variations on the order of 0.1 micrometer and spatial periods up to tens of micrometers. The patterns are caused by thermal expansion mismatch between the oxide and wafer when both are melted by the pulse. Damage can be completely avoided when the oxide thickness is greater than the depth of melt desired in the silicon, or when melting is avoided. Further experiments to quantify these observed effects are planned.

SECTION 4
FUTURE EXPERIMENTS

4.1 PULSED ELECTRON BEAM LIQUID EPITAXY (PEBLE)

Task 2 on this program is almost complete. The one additional experiment planned is to show the effect of an amorphous silicon layer compared to a polycrystalline silicon layer for pulsed epitaxial regrowth. It is believed[5] that better control of melt depth may be achieved with evaporated, sputtered, or implanted material. The experiment in progress has implanted some polycrystalline film (LPCVD) samples with 5×10^{15} Si/cm^2 at 50 keV. Melting has been observed at lower beam fluence, as inferred from optical changes. Analysis is continuing.

4.2 PULSED ELECTRON BEAM ANNEALING (PEBA)

Work reported to date has concentrated on optimization of the pulsed annealing schedule for low ion energy boron implants. As suggested in the program plan, experiments will be conducted with low energy arsenic and phosphorus implants, and high energy implants of As, B, and P at doses from 10^{12} to 10^{16} ions/cm^2. Measurement of the sheet resistance will be the principal diagnostic, with some etched mesa diodes formed to determine I-V and C-V characteristics. In addition, tests with implants through oxide masks or through thin oxide layers will be used to determine procedures for annealing devices.

4.3 DEVICE TESTING

This task has started on schedule with mesa etched diodes (Section 3.4) fabricated for initial tests. Other diode characteristics will be measured using Schottky barrier diodes (Section 4.3.1). Measurements of transistor properties will use JFET devices described in Section 4.3.2. Two types of structures will be used to determine whether there are any geometrical effects to PEBA using conventional sized resistors (Section 4.3.3) and an interdigitated pattern (Section 4.3.4).

4.3.1 Schottky Barrier Diodes

Schottky barrier diodes will be used to examine the type n on n^+ PEBLE films described in Section 2. Schottky diodes were chosen because they require no high temperature processing and can be totally nondestructive, thus allowing further use of the profiled material. Aluminum, gold, or mercury will make a good Schottky contact

with n-type silicon. A mercury probe will be used in the initial experiments. The current-voltage characteristics of the diode will be studied, and capacitance-voltage measurements using a Miller feedback profile plotter will provide information on the doping distribution in the lightly doped regrown n layer. Defect analysis of the film may be obtained by using these diodes for deep level transient capacitance measurements.

4.3.2 Junction Field Effect Transistors

Masks have been obtained for a ring-dot type of junction field effect transistor (JFET) (Figure 4-1). Since we are constrained by temperature limitations from using a thermal oxide for passivation, this structure, which will minimize surface effects, was chosen. This device will be used to test and evaluate the layers formed by the PEBLE process and PEBA ion implantation process, as well as to evaluate PEBA annealing of source, drain, and gate implantations. The source and drain contacts are phosphorus (n^+) implanted to assure low resistance ohmic contacts. The gate can be either ion implanted boron (p) or a Schottky barrier junction. Initially these FETs will be fabricated using conventional CVD epitaxy to form the channel. The pulsed electron beam will be used to anneal the source and drain contacts and the gate junction. When this process is under control, devices will be made on wafers which have the channel layers formed by pulsed electron beam epitaxy or by pulsed electron beam annealed ion implantation. These devices will be electrically characterized and evaluated. This device was chosen as a viable test vehicle under this program, since junction field effect transistors, particularly enhancement mode Schottky FETs, are being seriously considered for use in VLSI circuits.

4.3.3 Resistors

Ion implanted resistors are presently being processed in CVD epitaxial silicon, and later the same resistor test patterns will be used on PEBLE silicon (Figure 4-2). Pulsed electron beam annealing of the ion implantation damage will be used primarily, with some wafers annealed by conventional two step thermal processing for comparisons. Both resistance and capacitance measurements can be made on these devices as a function of process variables, to help optimize the pulsed electron beam annealing mechanisms. Stripe widths of 1.25, 2.5, 5, 12, and 50 micrometers will be used in the configurations shown in Figure 4-2. The resistor stripes will be implanted with 100 keV boron in four separate experiments at doses of $1 \times 10^{12}/cm^2$, $3 \times 10^{12}/cm^2$, $1 \times 10^{13}/cm^2$, and $3 \times 10^{13}/cm^2$. The contact pads will be implanted with 100 keV boron at a $3 \times 10^{14}/cm^2$ dose in all cases.

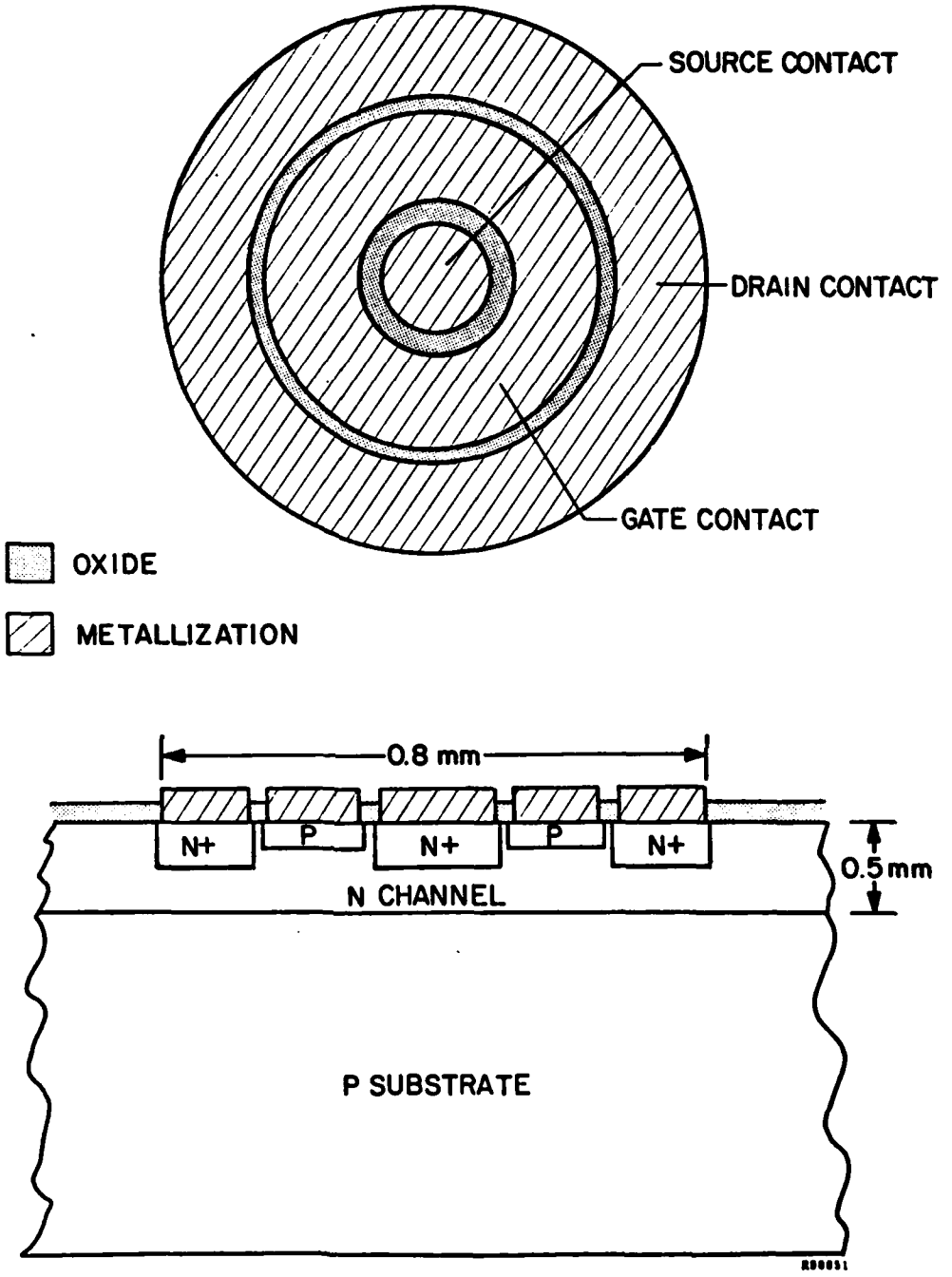


FIGURE 4-1. Ring-dot junction field effect transistor structure selected for testing pulsed electron beam annealing and epitaxy for device processing.

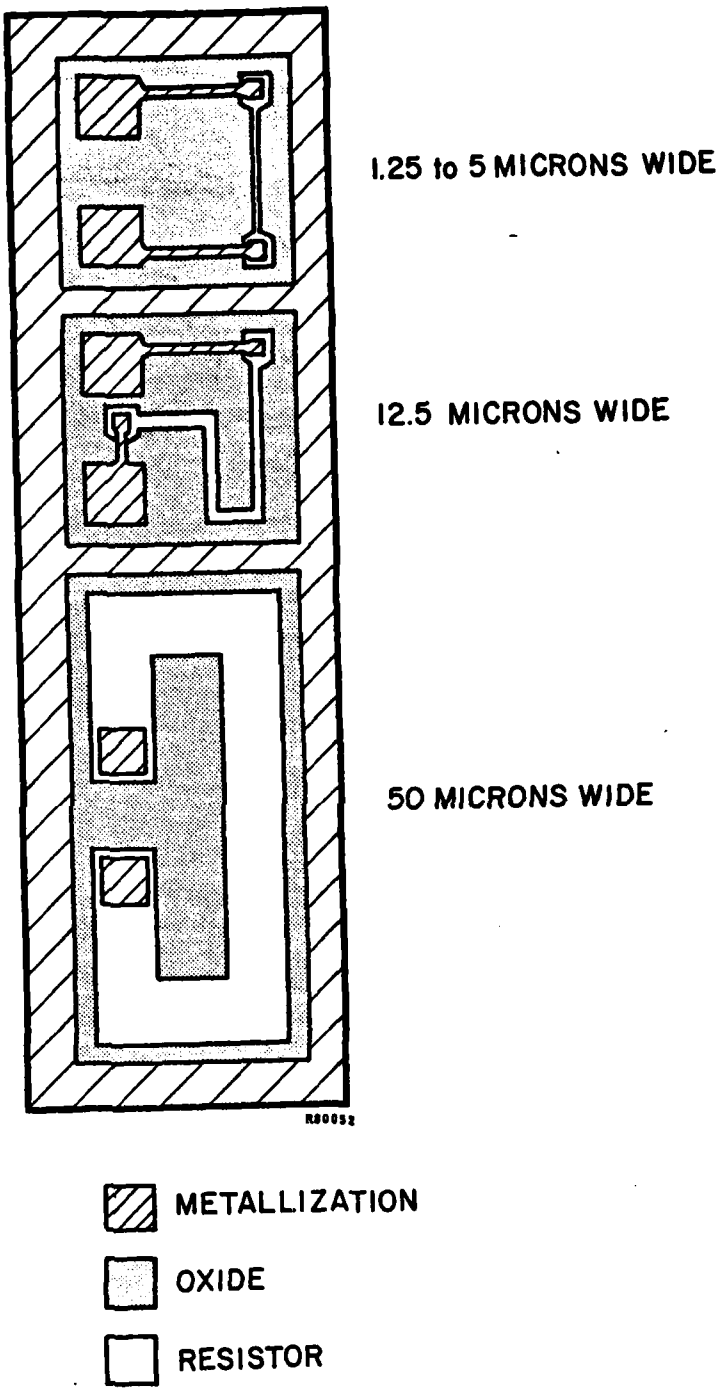


FIGURE 4-2. Ion implanted resistor test patterns for analyzing pulsed electron beam annealing with patterned oxides for device structures.

4.3.4 Linear Parallel Line Geometry

An interdigitated structure has been designed for determining lateral dopant motion during pulsed electron beam annealing of ion implanted structures (Figure 4-3). There will be four sets of wafers used in this experiment with each receiving 100 keV B^+ ion implantation of $1 \times 10^{12}/cm^2$, $3 \times 10^{12}/cm^2$, $1 \times 10^{13}/cm^2$, and $3 \times 10^{13}/cm^2$, respectively. Resistance variations among 20 ion implanted stripes, 2.5 micrometers wide and spaced 3.5 micrometers apart, will be determined as a function of annealing conditions. The investigation will include both pulsed electron beam annealed and thermally annealed samples, with and without oxide masks on the surface during annealing. Surface contamination studies will also be made in conjunction with this experiment.

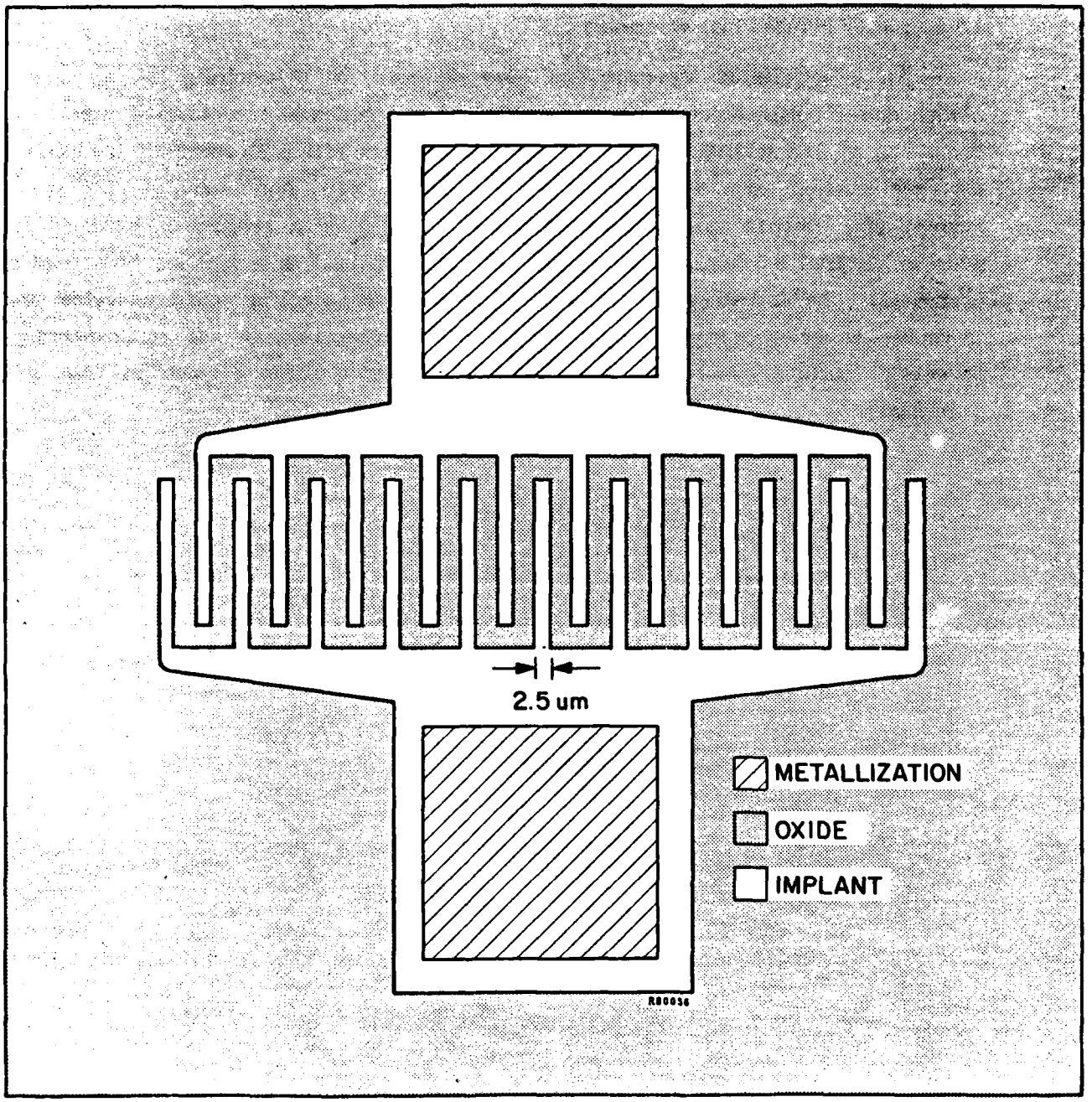


FIGURE 4-3. Parallel line structure to investigate lateral dopant motion during pulsed electron beam annealing.

REFERENCES

1. Martin L. Hammond, Solid State Technol. 21, 68 (Nov. 1978).
2. Billy L. Crowder, Ion Implantation in Semiconductors and Other Materials (Plenum Press, New York, 1973).
3. Leopoldo D. Yau, IEEE Trans. Electron. Devices ED-26, 1299 (1979).
4. A.C. Greenwald, A.R. Kirkpatrick, R.G. Little, and J.A. Minnucci, J. Appl. Phys. 50, 783 (1979).
5. A.C. Greenwald, first semiannual report on this contract (July 1979).
6. Reflected electron diffraction and electron channeling analysis was performed by J.J. Comer, RADC, Hanscom AFB, Massachusetts.
7. SIMS analysis was performed by Charles Evans, Associates, in California.
8. J.C. Beau, H.J. Leamy, J.M. Poate, G.A. Rozgonyi, J.P. van der Ziel, J.S. Williams, and G.K. Celler, J. Appl. Phys. 50, 881 (1979).
9. R.T. Young, J. Narayan, and R.F. Wood, Appl. Phys. Lett. 35, 447 (1979).
10. D.H. Auston, J.A. Golovchuka, A.L. Simons, C.M. Surko, and T.N.C. Venkentessen, Appl. Phys. Lett. 34, 777 (1979).
11. J.C. Brice, Solid-State Electron. 6, 673 (1963).
12. A.S. Grove, Physics and Technology of Semiconductors (John Wiley and Sons, New York, 1967).
13. P. Baeri, S.U. Campesan, G. Foto, and E. Riminic, Phys. Rev. Lett. 41, 1246 (1978).
14. John R. Dennis and Edward B. Hale, J. Appl. Phys. 49, 1119 (1978).
15. A. Gat, A. Lietoila, and J.F. Gibbons, J. Appl. Phys. 50, 2926 (1979), and other references therein.
16. K. Uda and M. Kamoshida, J. Appl. Phys. 48, 18 (1977).
17. Private communication, Glawischnig (Siemens).
18. J. S. Williams et al., Appl. Phys. Lett. 33, 542 (1978).
19. Experiments performed by S. Prussin at TRW in California (unpublished).
20. R. A. Street, N. M. Johnson, and J. F. Gibbons, J. Appl. Phys. 50, 8201 (1979).
21. T.I. Kamins and P. Rose, J. Appl. Phys. 50, 1308 (1979).